AMENDMENTS TO THE CLAIMS:

Please cancel claims 1 – 12 without prejudice or disclaimer of their subject matter.

This listing of claims will replace all prior versions and listings of claims in the application:

1. – 12. (Canceled)

13. (Original) A semiconductor device manufacturing method, comprising:

embedding an under interconnection layer in an interlayer insulating layer such that a surface thereof is exposed to substantially the same plane as a surface of said interlayer insulating layer;

forming a diffusion preventive layer to prevent diffusion of a metal included in said under interconnection layer, on at least said under interconnection layer;

forming a first nitrogen-doped silicon oxide layer on said diffusion preventive layer;

forming a fluorine-doped silicon oxide layer on said nitrogen-doped silicon oxide layer;

forming an interconnection groove and a via hole extending from a bottom of said interconnection groove above said under interconnection layer in said fluorine-doped silicon oxide layer; and

forming a plug in said via hole with a metal layer, to be in electrically contact with said under interconnection layer, and an upper interconnection layer in said interconnection groove with said metal layer, to be electrically contact with said plug.

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14. (Original) The semiconductor device manufacturing method according to claim 13, wherein said forming a first nitrogen-doped silicon oxide layer on said diffusion preventive layer includes setting a refractive index of said first nitrogen-doped silicon oxide layer to be 1.50 or more and 1.55 or less.

15. (Original) The semiconductor device manufacturing method according to claim 13, wherein said forming a first nitrogen-doped silicon oxide layer on said diffusion preventive layer includes setting a nitrogen concentration of said first nitrogen-doped silicon oxide layer to be 6 atomic % or more and 10.5 atomic % or less.

16. (Original) The semiconductor device manufacturing method according to claim 13, further comprising forming another diffusion preventive layer on at least said upper interconnection layer to prevent diffusion of a metal included in said upper interconnection layer.

17. (Original) The semiconductor device manufacturing method according to claim 13, wherein said interlayer insulating layer comprises a fluorine-doped silicon oxide layer.

18. (Original) The semiconductor device manufacturing method according to claim 13, further comprising, after said forming a fluorine-dopes silicon oxide layer on said first nitrogen-

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doped silicon oxide layer, forming a second nitrogen-doped silicon oxide layer on said fluorine doped silicon oxide layer,

wherein said forming an interconnection groove in said fluorine-doped silicon oxide layer includes forming said interconnection groove to penetrate said second nitrogen-doped silicon oxide layer.

19. (Original) The semiconductor device manufacturing method according to claim 18, wherein said forming a plug in said via hole and an upper interconnection layer in said interconnection groove includes forming said metal layer on said second nitrogen-doped silicon oxide layer having said interconnection groove and said via hole, with a thickness sufficient to fill up an interior of said interconnection groove and said via hole, followed by removing said metal layer over said second nitrogen-doped silicon oxide layer.

20. (Original) The semiconductor device manufacturing method according to claim 19, wherein said forming a plug in said via hole and an upper interconnection layer in said interconnection groove further includes removing said second nitrogen-doped silicon oxide layer and said metal layer formed over said fluorine-doped silicon oxide layer, after said removing said metal layer over said second nitrogen-doped silicon oxide layer.

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